UNIVERSITY OF ARIZONA

College of Engineering
Department of Electrical Engineering
Analog/Hybrid Computer Laboratory

Semiannual Progress Report for Period 3/15/66 to 9/15/66

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1. ASTRAC II Applications

The new ASTRAC II iterative differential analyzer was employed on three research projects dealing with significant applications of high-speed analog/hybrid computation. All three projects were completed on schedule during the summer.

(a) High-speed Analog-digital computer study of control-system optimization based on Pontryagin's Maximum Principle (Ph.D. Thesis, R. Maybach).

Abstract: Pontryagin's Maximum Principle affords a means of solving optimal control problems on a hybrid computer. For many minimum-time problems the Principle can be simplified due to the redundancy of the condition that the final value of the Hamiltonian be zero. The state and adjoint equations and control are simulated on analog computing elements. The Hamiltonian is maximized directly by steepest ascent without any need for iteration. A digital 4-parameter optimizer solves the troublesome two-point boundary-value problem at 1000 iterations per second. Several linear and nonlinear minimum-time control problems, including a case involving state-space constraints, were successfully treated.

(b) High-speed Monte-Carlo Technique for Hybrid-computer Solution of Partial Differential Equations (Ph.D. Thesis, H. Handler)

Abstract: The hybrid/analog-digital computer Monte-Carlo technique for solving elliptic and parabolic differential equations has been implemented on a new hybrid computer capable of taking statistics over 1,00 two- or three-dimensional random walks each second. This exceptional computing speed and flexible digital control permit direct plotting of partial-differential-equation solutions. The Monte-Carlo method has been extended to a wider class of boundary conditions especially applicable to heat conduction/diffusion problems. Another application has been to the solution of eigenvalue problems in vibration theory and quantum mechanics.

(c) Correlation Method for Computing Sensitivity Functions on a High-speed Iterative Analog Computer (E. P. O'Grady)

Abstract: During successive high-speed iterative-analog-computer runs, the parameters $a_1, a_2, \ldots, a_m$ of a simulated dynamical system are perturbed by mutually orthogonal binary sequences of perturbations $\Delta a_i = \pm \Delta a$. Each parameter perturbation remains constant during a full 1 msec analog-computer run. Simple correlation of the perturbed solution-sample sequences $x(t_k) + \Delta x(t_k)$ with each parameter-perturbation sequence simultaneously produces approximations $\Delta x(t_k)/\Delta a_i$ to all the system sensitivity coefficients $\partial x(t)/\partial a_i$ as the sampling time t_k is automatically stepped. Note that correlation with

binary variables requires no multipliers. The new technique is compared to the conventional method requiring separate sensitivity-equation setups for each sensitivity coefficient, and a simple example is presented.

The following short student term-paper projects were also completed:

Hirtz, J. A.: An Error Study for Cascaded Track/hold Circuits
Read, M.: Simulation of one-bit correlation on ASTRAC II
Liebert, T. A., and W. R. Stratton: The Use of Dither for Reduction of Quantization Error

As in earlier report periods, not all of the graduate students working with ASTRAC II were directly supported by the subject grant; this emphasizes, once again, how the sophisticated computing equipment completed under the NASA grant benefits, and will continue to benefit, students and research.

2. Combination of ASTRAC II with A Digital Computer

A grant supplement received early during the report period, together with some state matching funds, provides for a small general-purpose digital data processor for hybrid-computer applications. The choice of a specific machine was delayed until the WESCON conference because of the advent of new models and has narrowed down to essentially two computers: the short delay period to be an extremely wise one, because it will now be possible to obtain a 16-bit, 1μsec machine at little more than the cost of a 12-bit, 1.5 μsec computer earlier in the year. Software possibilities for small computers have been similarly improved, and it should now be possible to unite new hybrid programs in a FORTRAN-related language rather than simply in assembly language. A purchase decision will be made before October 1.

P. O'Grady's Ph.D. dissertation will involve digital control and statistics programs for problems which are extensions of R. Maybach's and R. Handler's thesis problems obtained above. The A/D/A linkage is completed, but the existing 8-bit D/A multipliers will be replaced by 12-bit D/A multipliers, since Maybach's results indicated a need for greater parameter resolution in optimization problems. The digital computer will permit much more sophisticated optimization routines and sequential estimation of statistics. Flow diagrams for such programs have been written; we hope to send one or two people to the digital-computer manufacturer's plant for additional programming instruction.

3. ASTRAC II Tests and Documentation

Complete ASTRAC II operator and maintenance manuals were completed during the summer and are now being typed. Complete test documentation and an account of the system design will be contained in H. Eckes's Ph.D. dissertation.

4. Hybrid-Computer Component and System Development: Digital-Attenuator System and LOCUST Project

(a) Digital Attenuator System (M.S. Thesis, C. Pracht)

A new system of digital-computer or keyboard controlled digital attenuators, intended to replace coefficient potentiometers in hybrid computers, was designed and one attenuator system is being breadboarded.

Although the new system employs bistable reed relays to control its low-impedance ladder networks, electronic bistable circuits control the relays. This will permit not only almost instantaneous setting of 100 to 300 attenuators, but also serial setting of each attenuator register, thus greatly simplifying the addressing circuits.

(b) LOCUST, an improved ASTRAC II-type system of radically lower cost, was supported by the subject grant only until June 1, 1966. The remainder of the project is being funded by an NSF summer grant to the Ph.D. candidate in question (B. Conant), by gifts of integrated circuits and amplifiers from Motorola and Burr-Brown, and with pieces of Engineering Experiment Station and Electrical Engineering Department funds. The Ph.D. dissertation is expected to be completed in Summer, 1967. Integrated-circuit logic for a complete small hybrid computer was designed and packaged on etched-circuit cards to be plugged directly into the computer patchbay. The prototype system, which uses Motorola MECL current-mode integrated-circuit logic, is at present being tested with a small educational hybrid computer (APE II). All sheet-metal work and component mounting for the digital portion of the final LOCUST computer system is also completed. Wide-band amplifiers and electronic switches for the analog-computer portion of the LOCUST system were started during the summer as M.S. thesis projects (A. Reames and J. Naylor).

5. Conference Participation and Publications

In June, 1966, the principal investigator presented accounts of our NASA-supported research to a seminar at the United Aircraft Research Center in Hartford, and to a meeting of the IEEE solid-state-circuits committee in New York; he also attended IBM's digital-simulation conference in Yorktown Heights, N. Y. as a guest of that company. He was an invited panel member at the Spring Joint Computer Conference in Boston and attended Simulation Councils, Inc. Summer Conference on Simulation at Breckenridge, Colorado.

The following reports were published or prepared:

1. Maybach, R. L.: Solution of Optimal-control Problems on a High-speed Hybrid Computer, Ph.D. Thesis, University of Arizona, September, 1966.

2. Handler, H.: High-speed Monte Carlo Technique for Hybrid-computer Solution of Partial Differential Equations, Ph.D. Thesis, University of Arizona, September, 1966.

3. O'Grady, E. P.: Correlation Method for computing Sensitivity Functions on a High-speed Iterative Analog Computer, ACL Memo No. 124, Electrical Engineering Department, University of Arizona, 1966 (submitted for publication).

4. Korn, G. A.: Design of a Modern Analog/Hybrid Computer for Laboratory Instruction (not supported by subject grant; invited paper for International Journal for Electrical Engineering Education; in print).

5. _____: Progress of Analog/Hybrid Computation (invited paper for special computer issue of Proc. IEEE, describes ASTRAC II, LOCUST, digital-attenuator projects; in print).

6. _____: Prospects for Engineering Simulation, ACL Memo No. 120, Electrical Engineering Dept., University of Arizona, 1966.

7. Eckes, H. R.: ASTRAC II Operator Manual (in print).

8. _____: ASTRAC II Maintenance Manual (in print).

A new report list is also being prepared. Finally, the following project reports prepared earlier were published in technical journals during the present report period:

1. O'Grady, E. P.: A Hybrid-code Differential Analyzer, Ann AICA, January, 1966 (Published in April, 1966).

2. Korn, G. A.: Reduction of Digital Noise in Hybrid Computers, Simulation, March, 1966 (published in April, 1966).